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02282.P055

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Raynaud et al.

Application No.: 09/127,584

Filed: July 31, 1998

For: METHOD AND APPARATUS FOR GATE-LEVEL SIMULATION OF SYNTHESIZED REGISTER TRANSFER LEVEL DESIGNS WITH SOURCE-LEVEL DEBUGGING

Examiner: Sergent, D.

Art Unit: 2763

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231 on:

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Signature: Heather Adamson Date: 6/1/00

Assistant Commissioner for Patents
Washington, D.C. 20231

AMENDMENT AND RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action mailed February 01, 2000, Applicant respectfully requests that the Examiner enter the following amendments and consider the following remarks.

IN THE SPECIFICATION

Please amend the specification as follows:

On page 6, line 23, please replace "Verilog" with --VHDL--.

On page 17, line 16, please replace "310" with --320--.

Atty. Docket No.: 02282.P055
Application No.: 09/127,584

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